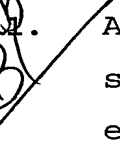## Claims

1. An interleaver (IL) for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits (e.g. I, Q for N=2) and control information (CI) consisting of a number L of control bits (e.g. FS, SS, MA, PW for L=4) indicating specific states for each code symbol; comprising:

   a) combining means (COM) for combining the respective N data bits (I, Q) of each code symbol with the associated L control bits (FS, SS, MA, PW) into a control information/code symbol data word of L+N bits;

   b) control information/code symbol encoding means (CI/CS-ENC) for encoding said L+N bit control information/code symbol data words into data words of K bits, where K<L+N, according to a predetermined encoding scheme; and

   c) an interleaving memory (IM) for storing said encoded data words at memory locations (IM00, IM01...) thereof.

2. An interleaver (IL) according to claim 1, further including a write/read means (W/R) for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations (IM00, IM01...) in a row direction and for reading out said encoded data words from said interleaving matrix

in the column direction and a control information/code symbol decoding means (CI/CS-DEC) for decoding said K bit data words read out from said interleaving matrix in said interleaving memory (IM) into said N bit code symbols and said L bit control bits (e.g. FS, SS, MA, PW) according to an inverse of said predetermined coding scheme.

3. An interleaver (IL) according to claim 1, wherein

L=4 and N=2, wherein said control bits (FS, SS, MA, PW) indicate a frame start (FS), a time slot start (SS), a marker (MA), a power bit (PW) for the code symbol consisting of said 2 data bits.

4. An interleaver (IL) according to claim 1, wherein

one control bit (PW) indicates a transmission power ON/OFF control (PW) of said code symbols.

5. An interleaver (IL) according to claim 2, wherein

each memory location (IM00, IM01...) stores one data word respectively consisting of said encoded combination of a predetermined number N of data bits selected from said input data bit sequence by a selection means (SM) of said write/read means (W/R) and said control bits.

6. An interleaver (IL) according to claim 1,
    wherein
    said input data bit sequence (BS) of M data bits
    consists of data bit sets each including a
    predetermined number $(1/r)$ of bits resulting from a
    convolutional encoding (CC) of a respective data bit
    using a predetermined coding rate (e.g. $r=1/2$) in a
    convolutional encoder (CC) preceding said interleaving
    memory (IM).

7. An interleaver (IL) according to claim 1,
    wherein
    said interleaving memory (IM) has N_W x N_R/K memory
    locations (IM00, IM01) for storing said the K data
    bits of the encoded data words, wherein N_W denotes the
    number of columns corresponding to the interleaving
    depth, K denotes the predetermined number of data bits
    forming one said data word and N_R/K denotes the number
    of rows in said interleaving memory.

8. An interleaver (IL) according to claim 2 ~~and 7~~,
    wherein
    said write/read means (W/R) comprises a selection
    means (SM) for building code symbols by selecting N
    respective data bits from the $[n_W + (n-1)N_W + n_R N_W \cdot N]$-
    th positions of the input data bit sequence, where n =
    1, 2...N denotes the n-th data bit of the code symbol,
    $n_W = 0, 1, ...N_W-1$ denotes the column address in the
    interleaving matrix and $n_R = 0, 1, ... (N_R/K)-1$ denotes
    the row address in the interleaving matrix of the data
    word resulting from a combining encoding of the code
    symbol and the additional control bits.

9.   An interleaver (IL) according to claim 8,
      wherein
      said selection means (SM) selects data bits for said
      code symbols from said input data bit sequence (BS)
      and provides said selected code symbol data bits to
      said combining means (COM) and comprises for N=2 data
      bits per code symbol and even N_W:

      -    two shift register banks (b0, b1) each consisting
           of a first and a second shift register (r0, r1)
           of length N_W, wherein the even and odd numbered
           data bits of said input data bit sequence are
           respectively stored in said first registers (r0)
           of said first and second shift register bank;

      -    select/write means (SW1, SW2) for selecting at
           each write cycle 2 data bits of the least
           significant bit position and the $N_W/2$ position
           from the first registers (r0) alternately from
           the first and second register bank and for
           providing said 2 selected bits as one code symbol
           to said combining means (COM) to be combined with
           said respective control bits;

      -    shift means (SHFT) for shifting the register (r0,
           r1) which was read at the last write cycle and
           the second registers of the register banks (b0,
           b1) while reading in the next odd and even bits
           of a next input data bit sequence to the
           respective second register (r1) of each register
           bank; and

-    wherein after N_W alternate data bit selecting and
     shifting cycles the function of the registers is
     reversed.

10. An interleaver (IL) according to claim 8,
     wherein
     said selection means (SM) selects data bits for said
     code symbols from said input data bit sequence (BS)
     and provides said selected code symbol data bits to
     said combining means (COM) and comprises for N=2 data
     bits per code symbol and odd N_W:

-    two shift register banks (b0, b1) each consisting
     of a first and a second shift register (r0, r1)
     of length N_W, wherein the even and odd numbered
     data bits of said input data bit sequence are
     respectively stored in said first registers (r0)
     of said first and second shift register bank;

-    select/write means (SM/RW) for selecting at each
     write cycle 2 data bits alternately either from
     the least significant bit position (LSB) of the
     first register of the first bank (b_0r_0) and from
     the central position ((N_W-1)/2) of the first
     register of the second bank b_1r_0 or from the
     central position of the first register of the
     first bank b_0r_0 and the least significant bit
     position (LSB) of the first register of the
     second bank (b_1r_0), and for writing said 2
     selected bits as one code symbol to a respective
     memory position in said interleaving memory;

shift means (SHFT) for shifting the two registers
(r0, r0) which were read at the last write cycle
and the registers of the register banks (b0, b1)
which were not read, while reading in the next
odd and even bits of a next input data bit
sequence to the respective second register (r1)
of each register bank; and

- wherein after N_W alternate data bit selecting and
shifting cycles the function of the registers
within each bank is reversed.

11. A transmitter for transmitting a data bit sequence
(BS) of M data bits comprising code symbols each
consisting of a number N of data bits (e.g. I, Q)
together with control information (CI) consisting of a
number L of control bits (e.g. FS, SS, MA, PW)
indicating specific states for each code symbol,
comprising:

a) combining means (COM) for combining the
respective N data bits (I, Q) of each code symbol
with the associated L control bits (FS, SS, MA,
PW) into a control information/code symbol data
word of L+N bits;

b) control information/code symbol encoding means
(CI/CS-ENC) for encoding said L+N control
information/code symbol data words into data
words of K bits, where K<L+N, according to a
predetermined encoding scheme;

.c) processing means (IL, MOD) for processing said
code symbols of said encoded data words in
accordance with their control information.

12. A transmitter (IL) according to claim 11,
said processing means (IL, MOD) further including a
modulation means (MOD) for modulating said decoded
code symbols in accordance to the specific state of
the code symbol as indicated by the respective control
bits.

13. A method for interleaving input data bit sequences
(BS) of M data bits comprising code symbols each
consisting of a number N of data bits (I, Q) together
with control information (CI) consisting of a number L
of control bits (FS, SS, MA, PW) indicating specific
states for each code symbol, comprising the following
steps:

a) combining the respective N data bits (e.g. I, Q
for N=2) of each code symbol with the associated
L control bits (e.g. FS, SS, MA, PW for L=4) into
a control information/code symbol data word of
L+N bits;

b) encoding said L+N bit control information/code
symbol data words into data words of K bits,
where K<L+N, according to a predetermined
encoding scheme; and

c) storing said encoded data words at memory
locations (IM00, IM01...) of a memory.

14. A method according to claim 13,
    further including the following steps:
    writing said encoded data words to an interleaving
    matrix within said interleaving memory at specific
    memory locations (IM00, IM01 ...) in a row direction
    and reading out said encoded data words from said
    interleaving matrix (IM) in the column direction and
    decoding said K bit data words read out from said
    interleaving matrix in said interleaving memory (IM)
    into said N bit code symbols and said L bit control
    bits (e.g. FS, SS, MA, PW) according to an inverse of
    said predetermined coding scheme.

15. A method according to claim 13,
    further including the following steps:
    processing decoded code symbols in accordance to the
    specific states of the code symbol as indicated by the
    respective control bits.

16. A method according to claim 13
    wherein
    L=4 and N=2, wherein said control bits (FS, SS, MA,
    PW) indicate a frame start (FS), a time slot start
    (SS), a marker (MA), a power bit (PW) for the code
    symbol consisting of said 2 data bits.

17. A method according to claim 13,
    wherein
    one control bit (PW) indicates a transmission power
    ON/OFF control (PW) of said code symbols.

18. A method for transmitting a data bit sequence (BS) of
    M data bits comprising code symbols each consisting of

a number N of data bits (e.g. I, Q for N=2) together
with control information (CI) consisting of a number L
of control bits (e.g. FS, SS, MA, PW for L=4)
indicating specific states for each code symbol,
comprising the following steps:

a)   combining the respective N data bits (e.g. I, Q
      for N=2) of each code symbol with the associated
      L control bits (e.g. FS, SS, MA, PW for L=4) into
      a control information/code symbol data word of
      L+N bits;

b)   encoding said L+N control information/code symbol
      data words into data words of K bits, where
      K<L+N, according to a predetermined encoding
      scheme;

c)   processing said code symbols of said encoded data
      words in accordance with their control
      information; and

d)   transmitting said processed code symbols.

19.   An encoder (ENC) of a transmitter for transmitting a
      data bit sequence (BS) of M data bits comprising code
      symbols each consisting of a number N of data bits
      (e.g. I, Q for N=2) together with control information
      (CI) consisting of a number L of control bits (e.g.
      FS, SS, MA, PW for L=4) indicating specific states for
      each code symbol, comprising:

a)   combining means (COM) for combining the
      respective N data bits (I, Q) of each code symbol

with the associated L control bits (FS, SS, MA, PW) into a control information/code symbol data word of L+N bits;

b)   control information/code symbol encoding means (CI/CS-ENC) for encoding said L+N bit control information/code symbol data words into data words of K bits, where K<L+N, according to a predetermined encoding scheme;

c)   processing means (IL, MOD) for processing said code symbols of said encoded data words in accordance with their control information.

20.   An interleaver (IL) for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits (e.g. I, Q for N=2) and control information (CI) consisting of a number L of control bits (e.g. FS, SS, MA, PW for L=4) indicating specific states for each code symbol; comprising:

a)   combining means (COM) for combining the respective N data bits (I, Q) of each code symbol with the associated L control bits (FS, SS, MA, PW) into a control information/code symbol data word of L+N bits;

b)   control information/code symbol encoding means (CI/CS-ENC) for encoding said L+N bit control information/code symbol data words into data words of K bits, where K<L+N, according to a predetermined encoding scheme; and

c)   an interleaving memory (IM) for storing said
      encoded data words at memory locations (IM00,
      IM01...) thereof; and

a write/read means (W/R) for writing said encoded data
words to an interleaving matrix within said
interleaving memory at specific memory locations
(IM00, IM01...) in a row direction and for reading out
said encoded data words from said interleaving matrix
in the column direction and a control information/code
symbol decoding means (CI/CS-DEC) for decoding said K
bit data words read out from said interleaving matrix
in said interleaving memory (IM) into said N bit code
symbols and said L bit control bits (e.g. FS, SS, MA,
PW) according to an inverse of said predetermined
coding scheme.

21.   An interleaver (IL) for interleaving input data bit
      sequences (BS) of M data bits comprising code symbols
      each consisting of a number N of data bits (e.g. I, Q
      for N=2) and control information (CI) consisting of a
      number L of control bits (e.g. FS, SS, MA, PW for L=4)
      indicating specific states for each code symbol;
      comprising:

      a)   combining means (COM) for combining the
            respective N data bits (I, Q) of each code symbol
            with the associated L control bits (FS, SS, MA,
            PW) into a control information/code symbol data
            word of L+N bits;

b)   control information/code symbol encoding means
       (CI/CS-ENC) for encoding said L+N bit control
       information/code symbol data words into data
       words of K bits, where K<L+N, according to a
       predetermined encoding scheme; and

c)   an interleaving memory (IM) for storing said
       encoded data words at memory locations (IM00,
       IM01...) thereof; and

a write/read means (W/R) for writing said encoded data
words to an interleaving matrix within said
interleaving memory at specific memory locations
(IM00, IM01...) in a row direction and for reading out
said encoded data words from said interleaving matrix
in the column direction and a control information/code
symbol decoding means (CI/CS-DEC) for decoding said K
bit data words read out from said interleaving matrix
in said interleaving memory (IM) into said N bit code
symbols and said L bit control bits (e.g. FS, SS, MA,
PW) according to an inverse of said predetermined
coding scheme, and wherein

each memory location (IM00, IM01...) stores one data
word respectively consisting of said encoded
combination of a predetermined number N of data bits
selected from said input data bit sequence by a
selection means (SM) of said write/read means (W/R)
and said control bits.

22. An interleaver (IL) for interleaving input data bit
      sequences (BS) of M data bits comprising code symbols
      each consisting of a number N of data bits (e.g. I, Q

for N=2) and control information (CI) consisting of a
number L of control bits (e.g. FS, SS, MA, PW for L=4)
indicating specific states for each code symbol;
comprising:

a)   combining means (COM) for combining the
      respective N data bits (I, Q) of each code symbol
      with the associated L control bits (FS, SS, MA,
      PW) into a control information/code symbol data
      word of L+N bits;

b)   control information/code symbol encoding means
      (CI/CS-ENC) for encoding said L+N bit control
      information/code symbol data words into data
      words of K bits, where K<L+N, according to a
      predetermined encoding scheme; and

c)   an interleaving memory (IM) for storing said
      encoded data words at memory locations (IM00,
      IM01...) thereof; and

a write/read means (W/R) for writing said encoded data
words to an interleaving matrix within said
interleaving memory at specific memory locations
(IM00, IM01...) in a row direction and for reading out
said encoded data words from said interleaving matrix
in the column direction and a control information/code
symbol decoding means (CI/CS-DEC) for decoding said K
bit data words read out from said interleaving matrix
in said interleaving memory (IM) into said N bit code
symbols and said L bit control bits (e.g. FS, SS, MA,
PW) according to an inverse of said predetermined
coding scheme, and wherein

said interleaving memory (IM) has N_W x N_R/K memory
locations (IM00, IM01) for storing said the K data
bits of the encoded data words, wherein N_W denotes the
number of columns corresponding to the interleaving
depth, K denotes the predetermined number of data bits
forming one said data word and N_R/K denotes the number
of rows in said interleaving memory; and

said write/read means (W/R) comprises a selection
means (SM) for building code symbols by selecting N
respective data bits from the $[n_W + (n-1)N_W + n_R N_W \cdot N]$-
th positions of the input data bit sequence, where n =
1, 2...N denotes the n-th data bit of the code symbol,
n_W = 0, 1,...N_W-1 denotes the column address in the
interleaving matrix and n_R = 0, 1,...(N_R/K)-1 denotes
the row address in the interleaving matrix of the data
word resulting from a combining encoding of the code
symbol and the additional control bits.

23. An interleaver (IL) for interleaving input data bit
sequences (BS) of M data bits comprising code symbols
each consisting of a number N of data bits (e.g. I, Q
for N=2) and control information (CI) consisting of a
number L of control bits (e.g. FS, SS, MA, PW for L=4)
indicating specific states for each code symbol;
comprising:

a) combining means (COM) for combining the
respective N data bits (I, Q) of each code symbol
with the associated L control bits (FS, SS, MA,

PW) into a control information/code symbol data word of L+N bits;

b)   control information/code symbol encoding means (CI/CS-ENC) for encoding said L+N bit control information/code symbol data words into data words of K bits, where $K<L+N$, according to a predetermined encoding scheme; and

c)   an interleaving memory (IM) for storing said encoded data words at memory locations (IM00, IM01...) thereof; and

a write/read means (W/R) for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations (IM00, IM01...) in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means (CI/CS-DEC) for decoding said K bit data words read out from said interleaving matrix in said interleaving memory (IM) into said N bit code symbols and said L bit control bits (e.g. FS, SS, MA, PW) according to an inverse of said predetermined coding scheme, and wherein

said interleaving memory (IM) has $N_W \times N_R/K$ memory locations (IM00, IM01) for storing said the K data bits of the encoded data words, wherein N_W denotes the number of columns corresponding to the interleaving depth, K denotes the predetermined number of data bits

forming one said data word and N_R/K denotes the number of rows in said interleaving memory; and

said write/read means (W/R) comprises a selection means (SM) for building code symbols by selecting N respective data bits from the $[n_W + (n-1)N_W + n_R N_W \cdot N]$-th positions of the input data bit sequence, where n = 1, 2...N denotes the n-th data bit of the code symbol, n_W = 0, 1,...N_W-1 denotes the column address in the interleaving matrix and n_R = 0, 1,...(N_R/K)-1 denotes the row address in the interleaving matrix of the data word resulting from a combining encoding of the code symbol and the additional control bits; and

said selection means (SM) selects data bits for said code symbols from said input data bit sequence (BS) and provides said selected code symbol data bits to said combining means (COM) and comprises for N=2 data bits per code symbol and even N_W:

- two shift register banks (b0, b1) each consisting of a first and a second shift register (r0, r1) of length N_W, wherein the even and odd numbered data bits of said input data bit sequence are respectively stored in said first registers (r0) of said first and second shift register bank;

- select/write means (SW1, SW2) for selecting at each write cycle 2 data bits of the least significant bit position and the $N_W/2$ position from the first registers (r0) alternately from the first and second register bank and for

providing said 2 selected bits as one code symbol
to said combining means (COM) to be combined with
said respective control bits;

- shift means (SHFT) for shifting the register (r0,
r1) which was read at the last write cycle and
the second registers of the register banks (b0,
b1) while reading in the next odd and even bits
of a next input data bit sequence to the
respective second register (r1)of each register
bank; and

- wherein after N_W alternate data bit selecting and
shifting cycles the function of the registers is
reversed.

24. An interleaver (IL) for interleaving input data bit
sequences (BS) of M data bits comprising code symbols
each consisting of a number N of data bits (e.g. I, Q
for N=2) and control information (CI) consisting of a
number L of control bits (e.g. FS, SS, MA, PW for L=4)
indicating specific states for each code symbol;
comprising:

a) combining means (COM) for combining the
respective N data bits (I, Q) of each code symbol
with the associated L control bits (FS, SS, MA,
PW) into a control information/code symbol data
word of L+N bits;

b) control information/code symbol encoding means
(CI/CS-ENC) for encoding said L+N bit control
information/code symbol data words into data

words of K bits, where K<L+N, according to a predetermined encoding scheme; and

c)   an interleaving memory (IM) for storing said encoded data words at memory locations (IM00, IM01...) thereof; and

a write/read means (W/R) for writing said encoded data words to an interleaving matrix within said interleaving memory at specific memory locations (IM00, IM01...) in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction and a control information/code symbol decoding means (CI/CS-DEC) for decoding said K bit data words read out from said interleaving matrix in said interleaving memory (IM) into said N bit code symbols and said L bit control bits (e.g. FS, SS, MA, PW) according to an inverse of said predetermined coding scheme, and wherein

said interleaving memory (IM) has N_W x N_R/K memory locations (IM00, IM01) for storing said the K data bits of the encoded data words, wherein N_W denotes the number of columns corresponding to the interleaving depth, K denotes the predetermined number of data bits forming one said data word and N_R/K denotes the number of rows in said interleaving memory; and

said write/read means (W/R) comprises a selection means (SM) for building code symbols by selecting N respective data bits from the $[n_W + (n-1)N_W + n_R N_W \cdot N]$-th positions of the input data bit sequence, where n =

1, 2...N denotes the n-th data bit of the code symbol,
n_W = 0, 1,...N_W-1 denotes the column address in the
interleaving matrix and n_R = 0, 1,...(N_R/K)-1 denotes
the row address in the interleaving matrix of the data
word resulting from a combining encoding of the code
symbol and the additional control bits; and

said selection means (SM) selects data bits for said
code symbols from said input data bit sequence (BS)
and provides said selected code symbol data bits to
said combining means (COM) and comprises for N=2 data
bits per code symbol and odd N_W:

- two shift register banks (b0, b1) each consisting
  of a first and a second shift register (r0, r1)
  of length N_W, wherein the even and odd numbered
  data bits of said input data bit sequence are
  respectively stored in said first registers (r0)
  of said first and second shift register bank;

- select/write means (SM/RW) for selecting at each
  write cycle 2 data bits alternately either from
  the least significant bit position (LSB) of the
  first register of the first bank (b_0r_0) and from
  the central position $((N_W-1)/2)$ of the first
  register of the second bank b_1r_0 or from the
  central position of the first register of the
  first bank b_0r_0 and the least significant bit
  position (LSB) of the first register of the
  second bank (b_1r_0), and for writing said 2

selected bits as one code symbol to a respective memory position in said interleaving memory;

- shift means (SHFT) for shifting the two registers (r0, r0) which were read at the last write cycle and the registers of the register banks (b0, b1) which were not read, while reading in the next odd and even bits of a next input data bit sequence to the respective second register (r1) of each register bank; and

- wherein after N_W alternate data bit selecting and shifting cycles the function of the registers within each bank is reversed.